

OFP-MM85QG-SR4C

400G OSFP SR4 Optical Transceiver

Features

- Support 100GBASE per lane in multimode fiber
- Hot-pluggable OSFP Type form factor
- Data rate up to 425Gbps (4x 106.25Gbps)
- Reach up to 100m on MMF(OM4)
- 850nm VCSEL laser and PIN receiver
- High speed I/O electrical interface (400GAUI-4)
- Single MPO-12-APC Receptacle Type
- Compliant to RoHS 6/6
- Compliant to 400G OSFP MSA and CMIS5.0
- Operating case temperature: 0 to +70°C

Absolute Maximum Ratings

| Parameters | Symbol | Min | Max | Units | Notes |
|-----------------------------|----------|------|-----|-------|-------|
| Case Operating Temperature | T_{OP} | 0 | 70 | °C | 1,2 |
| Power Supply Voltage | V_{CC} | -0.5 | 3.6 | V | |
| Storage Temperature Range | T_{ST} | -40 | 85 | °C | 1,2 |
| Operating Relative Humidity | RH | 5 | 85 | % | 1,2,3 |

Notes:

- 1.Absolute Maximum Ratings are those beyond which damage to the device may occur.
- 2.Between the Recommended Operating conditions and Absolute Maximum ratings, prolonged operation is not intended, and permanent device degradation may occur.
- 3.Non-condensing.

Optical Specification(General)

| Parameter | 400GBASE-SR4 |
|------------------|-----------------------------------|
| Application code | 400G-SR4 |
| Standard | IEEE Std 802.3db&IEEE Std 802.3ck |
| Data rate(Gb/s) | 425Gb/s |

Transmitter Optical Characteristics

| Parameter | 400GBaSE-SR4 | Unit | Note |
|--|--------------------------------|------------|------|
| Signaling rate, each lane (range) | 53.125 ± 100 ppm | GBd | |
| Modulation format | PAM4 | - | |
| Center wavelength (range) | 840~860 | nm | |
| RMS spectral width (max) | 0.6 | nm | 1 |
| Average launch power, each lane (max) | 4 | dBm | |
| Average launch power, each lane (min) | -4.6 | dBm | |
| Outer Optical Modulation Amplitude (OMA _{outer}), each lane (max) | 3.5 | dBm | |
| Outer Optical Modulation Amplitude (OMA _{outer}), each lane (min)for max(TECQ, TDECQ)≤1.8 dBor 1.8 < max(TECQ, TDECQ)≤4.4 dB | - 2.6 -4.4+max (TECQ,TDECQ) | dBm dBm | |
| Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max) | 4.4 | dB | |
| Transmitter eye closure for PAM4 (TECQ), each lane (max) | 4.4 | dB | |
| Overshoot/undershoot (max) | 29 | % | |
| Transmitter power excursion, each lane (max) | 2.3 | dBm | |
| Extinction Ratio | 2.5 | dB | |
| Transmitter transition time, each lane (max) | 17 | ps | |
| Average launch power of OFF transmitter, each lane (max) | -30 | dBm | |
| RIN _{12OMA} (max) | - 132 | dB/Hz | |
| Optical return loss tolerance (max) | 14 | dB | |
| Encircled flux | ≥86% at 19 nm ≤30% at 4.5um | - | 2 |

Notes:

- 1.RMS spectral width is the standard deviation of the spectrum
- 2.If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280- 1-4

Receiver Optical Characteristics

| Parameter | 400GBASE-SR4 | Unit | Note |
|---|-------------------|------------|------|
| Signaling rate, each lane (range) | 53.125 ± 100 ppm | GBd | |
| Modulation format | PAM4 | - | |
| Center wavelength (range) | 840~860 | nm | |
| Damage threshold (min) | 5 | dBm | 1 |
| Average receive power, each lane (max) | 4 | dBm | |
| Average receive power, each lane (min) | -6.4 | dBm | 2 |
| Receive power, each lane (OMA _{outer}) (max) | 3.5 | dBm | |
| Receiver reflectance (max) | - 12 | dB | |
| Receiver sensitivity (OMA _{outer}), each lane (max) for TECQ≤1.8 dBfor 1.8<TECQ≤4.4 dB | -4.6 -6.4+TECQ | dBm dBm | |
| Stressed receiver sensitivity (OMA _{outer}), each lane (max) | -2 | dBm | 3 |
| Conditions of stressed receiver sensitivity test | | | 4 |
| Stressed eye closure for PAM4 (SECQ), lane under test | 4.4 | dB | |
| OMA _{outer} of each aggressor lane | 3.5 | dBm | |

Notes:

- 1.The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
- 2.Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
- 3.Measured with conformance test signal at TP3 (see 167.8.13) for the BER specified in 167.1.1.
- 4.These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Transmitter Electrical Characteristics

| Parameter | Reference | Value | Unit | |
|--|------------|------------------|------|---|
| Signaling rate, each lane (range) | 120G.3.4.1 | 53.125 ± 50 ppm | GBd | |
| Differential pk-pk input voltage tolerance (min) | 120G.5.1 | 900 | mV | |
| Differential to common-mode return loss (min) | 120G.3.3.2 | Equation(120G-2) | dB | |
| Effective return loss, ERL (min) | 120G.3.4.3 | 8.5 | dB | |
| Differential termination mismatch (max) | 120G.3.1.3 | 10 | % | |
| Module stressed input test | 120G.3.4.2 | See 120G.3.4.2 | | 1 |
| Single-ended voltage tolerance range (min) | 120G.5.1 | -0.4 to 3.3 | V | |
| DC common-mode voltage (min) | 120G.5.1 | -350 | mV | 2 |
| DC common-mode voltage (max) | 120G.5.1 | 2850 | mV | 2 |

Notes:

- 1.Meets BER specified in 120G.1.1 References are from IEEE 802.3ck
- 2.DC common-mode voltage generated by the host. Specification includes effects of ground offset voltage.

Receiver Electrical Characteristics

| Parameter | Reference | Value | Unit | Note |
|---|------------|-----------------------|----------|------|
| Signaling rate, each lane (nominal) | | 53.1251 | GBd | 1 |
| AC common-mode output voltage (max, RMS) | 120G.5.1 | 17.5 | mV | |
| Differential peak-to-peak output voltage (max) Short mode Long mode | 120G.5.1 | 600 900 | mV mv | |
| Eye height (min) | 120G.3.2.2 | 15 | mV | |
| Vertical eye closure, VEC (max) | 120G.3.2.2 | 12 | dB | |
| Common-mode to differential return loss (min) | 120G.3.1.1 | Equation (120G- 1) | dB | |
| Effective return loss, ERL (min) | 120G.3.2.3 | 8.5 | dB | |
| Differential termination mismatch (max) | 120G.3.1.3 | 10 | % | |
| Transition time (min) | 120G.3.1.4 | 8.5 | ps | |
| DC common-mode voltage (min) | 120G.5.1 | -350 | mV | 2 |
| DC common-mode voltage (max) | 120G.5.1 | 2850 | mV | 2 |

Notes:

- 1.The signaling rate range is derived from the PMD receiver input.
- 2.DC common-mode voltage is generated by the host. Specification includes effects of ground offset voltage.

Electrical Power Supply Characteristics

| Parameter | Symbol | Min | Typ. | Max | Units |
|---------------------------|---------------------------|------|------|------|-------|
| Power Supply Voltage | VCC1 , VCCTx, VCCRx | 3.13 | 3.30 | 3.47 | V |
| Power Consumption | PW | - | - | 10 | W |
| Power Consumption-LP mode | - | - | - | 1.5 | W |

Notes:The specified characteristics are met within the recommended range of operation. Unless otherwise noted typical data are quoted at nominal voltage and +25°C ambient temperature.

Electrical Pin Definition

| Pin | Symbol | Description | Logic | Direction | Plug Sequence | Note |
|-----|-----------|---------------------------------|-------------|-----------------|---------------|--|
| 1 | GND | Ground | | | 1 | |
| 2 | TX2p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 3 | TX2n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 4 | GND | Ground | | | 1 | |
| 5 | TX4p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 6 | TX4n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 7 | GND | Ground | | | 1 | |
| 8 | TX6p | Underfined | CML-I | Input from Host | 3 | |
| 9 | TX6n | Underfined | CML-I | Input from Host | 3 | |
| 10 | GND | Ground | | | 1 | |
| 11 | TX8p | Underfined | CML-I | Input from Host | 3 | |
| 12 | TX8n | Underfined | CML-I | Input from Host | 3 | |
| 13 | GND | Ground | | | 1 | |
| 14 | SCL | 2-wire Serial interface clock | LVC MOS-I/O | Bi-directional | 3 | Open-Drain with pull up resistor on H |
| 15 | VCC | +3.3V Power | | Power from Host | 2 | |
| 16 | VCC | +3.3V Power | | Power from Host | 2 | |
| 17 | LPWn/PRSn | Low-Power Mode / Module Present | Multi-Level | Bi-directional | 3 | See pin description for required circuit |
| 18 | GND | Ground | | | 1 | |
| 19 | RX7n | Underfined | CML-O | Output to Host | 3 | |
| 20 | RX7p | Underfined | CML-O | Output to Host | 3 | |
| 21 | GND | Ground | | | 1 | |
| 22 | RX5n | Underfined | CML-O | Output to Host | 3 | |
| 23 | RX5p | Underfined | CML-O | Output to | 3 | |
| 24 | GND | Ground | | | 1 | |
| 25 | RX3n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 26 | RX3p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 27 | GND | Ground | | | 1 | |
| 28 | RX1n | Receiver Data Inverted | CML-O | Output to Host | 3 | |

| | | | | | | |
|----|----------|---------------------------------|-------------|-----------------|---|--|
| 29 | RX1p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 30 | GND | Ground | | | 1 | |
| 31 | GND | Ground | | | 1 | |
| 32 | RX2p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 33 | RX2n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 34 | GND | Ground | | | 1 | |
| 35 | RX4p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 36 | RX4n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 37 | GND | Ground | | | 1 | |
| 38 | RX6p | Underfined | CML-O | Output to Host | 3 | |
| 39 | RX6n | Underfined | CML-O | Output to Host | 3 | |
| 40 | GND | Ground | | | 1 | |
| 41 | RX8p | Underfined | CML-O | Output to Host | 3 | |
| 42 | RX8n | Underfined | CML-O | Output to Host | 3 | |
| 43 | GND | Ground | | | 1 | |
| 44 | INT/RSTn | Module Interrupt / Module Reset | Multi-Level | Bi-directional | 3 | See pin description for required circuit |
| 45 | VCC | +3.3V Power | | Power from Host | 2 | |
| 46 | VCC | +3.3V Power | | Power from Host | 2 | |
| 47 | SDA | 2-wire Serial interface data | LVC MOS-I/O | Bi-directional | 3 | Open-Drain with pull up resistor on Host |
| 48 | GND | Ground | | | 1 | |
| 49 | TX7n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 50 | TX7p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 51 | GND | Ground | | | 1 | |
| 52 | TX5n | Underfined | CML-I | Input from Host | 3 | |
| 53 | TX5p | Underfined | CML-I | Input from Host | 3 | |
| 54 | GND | Ground | | | 1 | |
| 55 | TX3n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 56 | TX3p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 57 | GND | Ground | | | 1 | |
| 58 | TX1n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |

| | | | | | | |
|----|------|-------------------------------|-------|-----------------|---|--|
| 59 | TX1p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 60 | GND | Ground | | | 1 | |

Connector Pad Layout

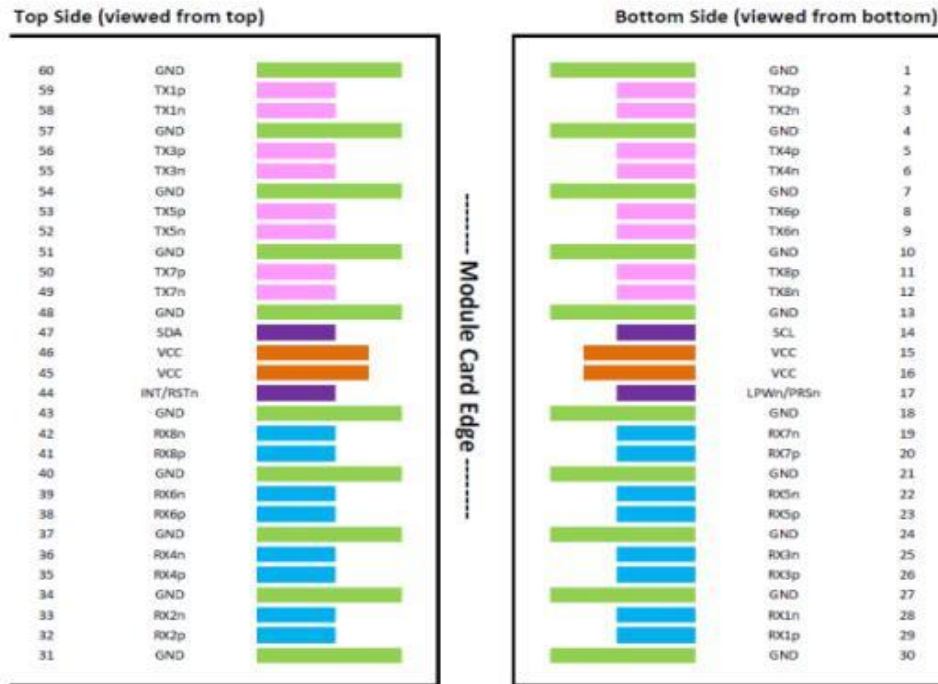


Figure 11-1: OSFP module pinout

Figure 1 OSFP Module contact assignment

Application Notes

Electrical interface: All signal interfaces are compliant with the OSFP REV4.1 MSA specification. The high speed DATA interface is differential AC-coupled internally and can be directly connected to a 3.3V SERDES IC.

High-Speed Signals: The high-speed signals consist of 4 transmit and 4 receive differential pairs identified as TX[4:1]p / TX[4:1]n and RX[4:1]p/RX[4:1]n. These signals can be operated in port configurations of either a single 4-lanes, dual 2-lanes, 4 individual lanes depending on the capability of the host ASIC.

400GAUI-4 mode provides 4 differential lanes using 112G-PAM4 signaling operating at 53.125 GBaud.

This results in 4 lanes of 100Gb/s for a total of 400Gb/s.

The high-speed signals follow the electrical specifications of IEEE802.3bs, IEEE802.3cd, IEEE802.3ck and CEI-56G-VSR-PAM as defined in OIF-CEI-04.0 for 400GAUI-4 mode and IEEE802.3bj, IEEE802.3bm for CAUI-4 mode.

Low-Speed Signals: There are 4 low-speed signals consisting of SCL, SDA, LPWn/PRSn and INT/RSTn. These signals are used for configuration and control of the module by the host. SCL and SDA use 3.3V LVCMOS levels and are bidirectional signals. LPWn/PRSn and INT/RSTn have additional circuitry on the host and module to enable multi-level bidirectional signaling.

Power: +3.3V power is delivered to the module via 4 power pins (VCC). These 4 power pins shall be connected together on the module and also together on the host. Each power pin allows up to 2.5 Amps for a total of 10.0 Amps. This enables a maximum power in excess of 30 Watts.

The specification of the module power is in accordance with methods defined by SFF- 8679 Rev 1.7 section 5.5. There are 8 power classes defined as shown in Table 11-8. All modules in reset or the default low power mode must comply with Power Class 1. High power mode enables the module to draw power up to its advertised power class, and may be conditionally enabled by the host. The host may read the module power class register to know the power class of the module before or after enabling high power mode. The module shall not exceed the power class it identifies for itself.

Transition between low and high power mode is controlled by the M_RSTn (reset) signal, M_LPWn (low power mode) signal and ForceLowPwr bit. The module shall remain in or transition to low power mode when M_LPWn or M_RSTn are asserted or the ForceLowPwr bit is set. While in low power mode, active modules shall also disable transmitters. The module may transition to high power mode once M_RSTn and M_LPWn are deasserted and the ForceLowPwr bit is cleared.

Digital Diagnostic Specification

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|-----------|-------|---------|------|-------|----------------------|
| Transceiver Case Temperature | DMI_Temp | -3 | | +3 | °C | Over operating temp |
| Supply voltage monitor absolute error | DMI_VCC | -3% | | +3% | V | Full operating range |
| Channel RX power monitor absolute error | DMI_RX | -3 | | +3 | dB | Per channel |
| Channel Bias current monitor | DMI_Ibias | - 10% | | +10% | mA | Per channel |
| Channel TX power monitor absolute error | DMI_TX | -3 | | +3 | dB | Per channel |

Memory Map-5.0

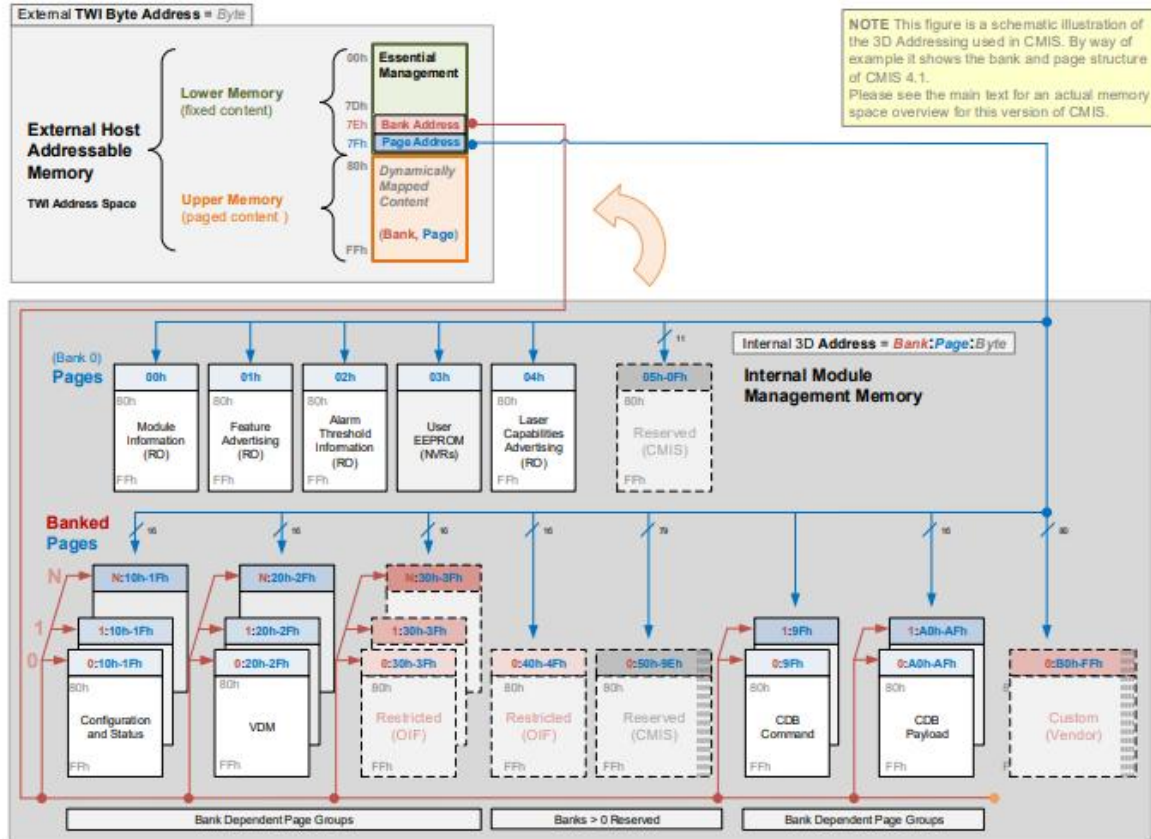


Figure 3 - OSFP Memory Map

OPTICAL INTERFACE LANES AND ASSIGNMENT

The recommended location and numbering of the optical ports for 3 Media Dependent Interfaces (MDI) are shown in Figure 4. The transmit and receive optical lanes shall occupy the positions depicted in Figure 4 when looking into the MDI receptacle with the connector keyway feature on top.

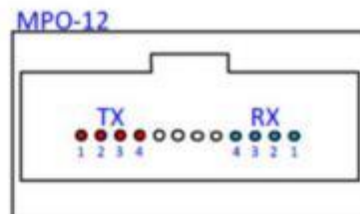


Figure 4 -Optical media dependent interface port assignment

Mechanical Specifications

All dimensions shown are in millimetres.

Tolerances are in accordance with OSFP MSA.

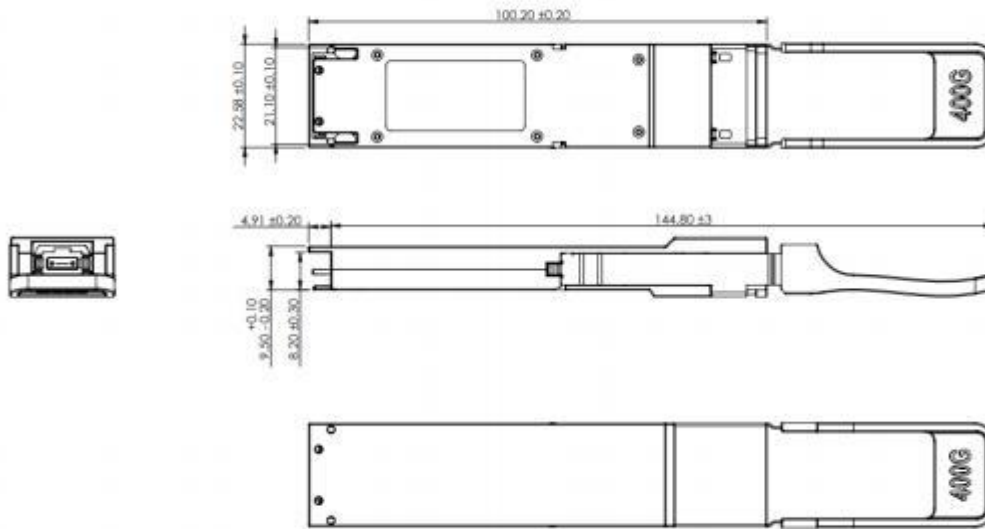


Figure 5 – OSFP Mechanical Specifications

Ordering information

| Part Number | Product Description |
|-----------------|--|
| OFP-MM85QG-SR4C | 400Gbps, OSFP SR4 , 850nm, 100m, 0°C~+70°C |

For More Information

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